16-bit Fully Differential Input 2/1 MSPS SAR ADC

Features

- 16-bit Fully Differential Input
- Throughput:
  - ZJC2400-16 up to 2 MSPS
  - ZJC2401-16 up to 1 MSPS
- INL: ±0.4 LSB
- DNL: ±0.25 LSB
- SINAD: 95.5 dB at 1 kHz
- THD: -115 dB at 1 kHz
- Pseudo Differential Input Range: 0 V ~ V_{REF}
- External Reference Range V_{REF} = 2.4 V ~ 5.1 V
- Single Analog Supply V_{DD} = 1.8 V
- 1.8 V/2.5 V/3 V/5 V Logic Interface
- Packages: MSOP-10/DFN-10

Applications

- Precision Data Acquisition
- Automated Testing
- Precision Instrument
- Medical Instrument

General Description

ZJC2400-16 is low noise, low power consumption, 16-bit pseudo differential SAR ADC with throughput up to 2 MSPS (ZJC2401-16 is up to 1 MSPS). The part is available in small package and easy to use. It can reduce the power consumption and complexity of the system, thus achieve high density designs.

ZJC2400/1-16 requires typically 1.8 V of power supply. The reference voltage of ZJC2400/1-16 should be provided externally to sample the analog input voltage between IN+ and IN- ranging from -V_{REF} to +V_{REF} (V_{REF}: 2.4 V to 5.1 V). Utilizing the independent V_{IO} pin, ZJC2400/1-16 can be compatible with 1.8 V, 2.5 V, 3.3 V and 5 V logic interface. The part provides one SPI-compatible serial port and also supports daisy-chain operation for serial cascading of multiple devices.

ZJC2400/1-16 is available in 10-lead MSOP and DFN packages. The operating temperature is -40 °C to +125 °C.

Typical Application

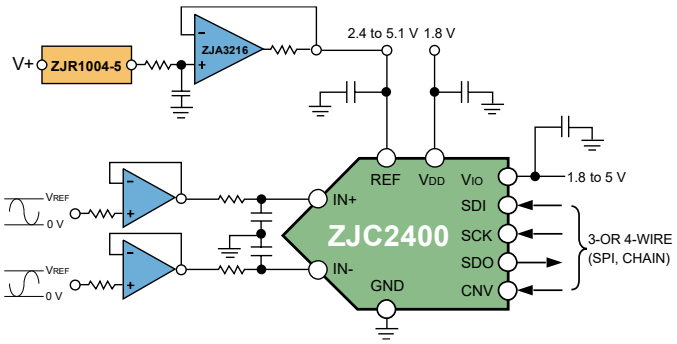

Figure 1. Application Examples

Typical Characteristics

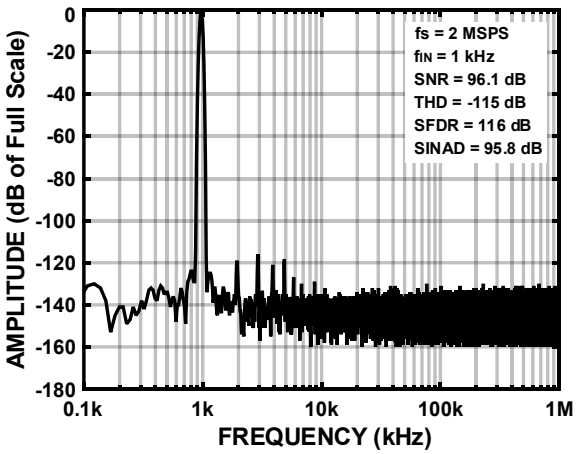

Figure 2. AC Characteristics

18/16-bit high speed SAR ADC ZJC2400 series is listed below:

Model	2 MSPS	1 MSPS	Packages
18-bit Fully Differential	ZJC2400-18	ZJC2401-18	MSOP-10 DFN-10
18-bit Unipolar Pseudo Differential	ZJC2402-18	ZJC2404-18	
16-bit Fully Differential	ZJC2400-16	ZJC2401-16	
16-bit Unipolar Pseudo Differential	ZJC2402-16	ZJC2404-16	

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Version (Preliminary Datasheet) [1]

Nov. 2025 — Preliminary Datasheet

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Pin Configurations and Function Descriptions

Figure 3. 10-lead MSOP pin configuration

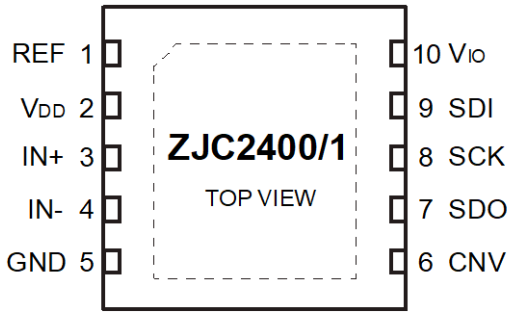

Figure 4. 10-lead DFN pin configuration

Note: The exposed pad has no internal connection. Connect the pad to GND.

Mnemonic	Pin No.	Pin Type [1]	Description
REF	1	P	The voltage reference input. V_{REF} ranges from 2.4 V to 5.1 V. It is recommended that this pin must be decoupled to the GND by a 10 or 22 µF X7R ceramic capacitor as close as possible.
V_{DD}	2	P	Power Supply pin. V_{DD} ranges from 1.71 V to 1.89 V. It is recommended that V_{DD} be bypassed through a minimum of 0.1 µF and 10 µF ceramic capacitor to GND.
IN+	3	AI	Analog input positive pin. IN+ to GND ranges from 0 V to V_{REF}. IN+ and IN- form a pseudo differential input with an input range of 0 V to V_{REF}.
IN-	4	AI	Analog input negative pin. IN- to GND ranges from V_{REF} to 0 V. IN+ and IN- form a fully differential input with an input range of -V_{REF} to V_{REF}.
GND	5	GND	Power Ground.
CNV	6	DI	Conversion input. This input has multiple functions as described in the Digital Interface section.
SDO	7	DO	Serial data output. The conversion result is output through this pin. It is synchronized with SCK.
SCK	8	DI	Serial data clock input. When the device is selected, the conversion result is shifted out through this clock.
SDI	9	DI	Serial data input. This input provides multiple functions to implement a variety of different serial protocols
V_{IO}	10	P	Input/output interface digital power supply. The nominal voltage on this pin is the same as the controller interface power supply (1.8 V, 2.5 V, 3.3 V, or 5 V). It is recommended that VIO be bypassed through a minimum of 0.1 µF ceramic capacitor to GND.

[1] AI/O: Analog Input or Output; P: Power; DI/O: Digital Input or Output; GND: Ground.

Absolute Maximum Ratings [1]

Parameter	Rating
V_{DD} to GND	-0.3 V ~ +2.1 V
REF, VIO to GND	-0.3 V ~ +6 V
V_{DD} to V_{IO}	-6 V ~ +2.4 V
Analog Input Range (IN+, IN- to GND)	-0.3 V ~ REF +0.3 V or ±130 mA (10 ms)
Digital Input to GND	-0.3 V ~ V_{IO} + 0.3 V
Digital Output to GND	-0.3 V ~ V_{IO} + 0.3 V
Storage Temperature Range	-65 °C to +150 °C
Junction Temperature Range	150 °C
Lead Temperature (Soldering, 10 seconds)	300 °C
Maximum Reflow Temperature [2]	260 °C
Electrostatic Discharge (ESD) [3]	
Human Body Model (HBM) [4]	2 kV
Charged Device Model (CDM) [5]	1 kV

Thermal Resistance [6]

Package Type	θ_{JA}	θ_{JC}	Unit
MSOP-10	150	50	°C/W
DFN-10	43	5.5	°C/W

[1] These ratings apply at 25 °C, unless otherwise noted. Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not implied.

[2] IPC/JEDECJ–STD-020 Compliant.

[3] Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

[4] ANSI/ESDA/JEDEC JS-001 Compliant.

[5] ANSI/ESDA/JEDEC JS-002 Compliant.

[6] θ_{JA} addresses the conditions for soldering devices onto circuit boards to achieve surface mount packaging.

Specifications

The ● denotes the full temperature range for specified performance.

Unless otherwise noted, V_{DD} = 1.71 V ~ 1.89 V, V_{IO} = 1.71 V ~ 5.5 V, V_{REF} = 5 V, T_A = 25 °C.

Parameter	Symbol	Conditions		Min	Typ.	Max	Unit
Resolution							
				16			bits
Input Characteristics							
Voltage Range		IN+ to IN-	●	$-V_{REF}$		$+V_{REF}$	V
Absolute input voltage		IN+, IN -	●	-0.1		V_{REF} + 0.1	V
Common Mode Input Range		IN+, IN-	●	V_{REF}/2 - 0.1	V_{REF}/2	V_{REF}/2 + 0.1	V
Common Mode Rejection Ratio	CMRR	f_{IN} = 500 kHz			65		dB
Throughput							
Conversion Rate		ZJC2400-16	●			2	MSPS
		ZJC2401-16	●			1	MSPS
Transient Response		Full-scale Step	●			225	ns
DC Accuracy							
No Missing Codes			●	16			bits
Integral Nonlinear Error	INL	V_{REF} = 5 V, V_{DD} = 1.8 V	●		±0.4		LSB [2]
Differential Nonlinear Error	DNL	V_{REF} = 5 V, V_{DD} = 1.8 V	●		±0.25		LSB
Transition Noise		V_{REF} = 5 V, V_{DD} = 1.8 V	●		0.35		LSB
Power Supply Sensitivity		V_{DD} = 1.8 V ± 5%			±0.3		LSB
1/f Noise		Bandwidth = 0.1 Hz to 10 Hz			6		μV_{P-P}
AC Accuracy							
Dynamic Range	DR	V_{REF} = 5 V	●		96.1		dB [1]
Total RMS Noise		V_{REF} = 5 V			55		μVrms
f_{IN} = 1 kHz, V_{REF} = 5 V	SNR		●	95	96		dB
	SFDR				116		dB
	THD				-115		dB
	SINAD		●		95.5		dB
f_{IN} = 1 kHz, V_{REF} = 2.5 V	SNR		●	92	93		dB
	SFDR				115		dB
	THD				-113		dB
	SINAD		●		92.5		dB

[2] LSB means least significant bit. 1 LSB=153 μV for ±5 V input range.

[1] Unless otherwise noted, all specifications expressed in decibels (dB) are referenced to full-scale input FSR and are tested with an input signal 0.5 dB below full-scale.

Parameter	Symbol	Conditions		Min	Typ.	Max	Unit
f_{IN} = 100 kHz, V_{REF} = 5 V	SNR		●		95.2		dB
	SFDR				101		dB
	THD				-100		dB
	SINAD		●		95		dB
Reference							
Voltage Range			●	2.4		5.1	V
Sampling Dynamics							
-3 dB Input Bandwidth		V_{DD} = 1.8 V			10		MHz
Aperture Delay		V_{DD} = 1.8 V			3		ns
Digital Input							
Logic Level	V_{IL}	V_{IO} > 2.7 V	●	-0.3		0.3 x V_{IO}	V
		V_{IO} ≤ 2.7 V	●	-0.3		0.2 x V_{IO}	V
	V_{IH}	V_{IO} > 2.7 V	●	0.7 x V_{IO}		V_{IO} + 0.3	V
		V_{IO} ≤ 2.7 V	●	0.8 x V_{IO}		V_{IO} + 0.3	V
	I_{IL}		●	-1		+1	µA
	I_{IH}		●	-1		+1	µA
Digital Output							
Data Format				Serial 16-bit, twos complement			
Pipeline Delay				Upon the conversion is complete, the code is ready for reading			
	V_{OL}	I_{OUT} = +200 µA	●			0.4	V
	V_{OH}	I_{OUT} = -200 µA	●	V_{IO} - 0.3			V
Power Supplies							
Analog Power	V_{DD}		●	1.71	1.8	1.89	V
Digital Interface Power	V_{IO}		●	1.71		5.5	V
Stand-by Current		V_{DD} = 1.8 V, V_{IO} = 5 V, T = 25 °C			2		µA
Power Consumption		V_{DD} = 1.8 V, V_{IO} = 5 V, T = 25 °C					
Temperature Range							
Specified Performance		T_{MIN} to T_{MAX}		-40		+125	°C

Timing Specifications

The ● denotes the full temperature range for specified performance.

Unless otherwise specified, V_{DD} = 1.71 V ~ 1.89 V, V_{IO} = 1.71 V ~ 5.5 V, V_{REF} = 5 V, T_A = 25 °C.

Parameter	Symbol		Min	Typ.	Max	Unit
Conversion Time: CNV Rising Edge to Data Available	t_{CONV}	●			315	ns
Acquisition Time (ZJC2400-16)	t_{ACQ}	●	225			ns
Acquisition Time (ZJC2401-16)	t_{ACQ}	●	725			ns
Time Between Conversions (ZJC2400-16 Turbo Mode)	t_{CYC}	●	500			ns
Time Between Conversions (ZJC2400-16)	t_{CYC}	●	555			ns
Time Between Conversions (ZJC2401-16)	t_{CYC}	●	1000			ns
CNV Pulse Width ($\overline{CS}$ Mode)	t_{CNVH}	●	10			ns
SCK Period ($\overline{CS}$ Mode)	t_{SCK}	●				
V_{IO} > 2.7 V		●	10			ns
V_{IO} > 1.7 V		●	20			ns
SCK Period (Daisy-Chain Mode)	t_{SCK}	●				
V_{IO} > 2.7 V		●	20			ns
V_{IO} > 1.7 V		●	40			ns
SCK Low Time	t_{SCKL}	●	4			ns
SCK High Time	t_{SCKH}	●	4			ns
SCK Falling Edge to Data Remain Valid	t_{HSDO}	●	4			ns

Typical Performance Characteristics

Unless otherwise noted, V_{DD} = 1.8 V, REF = 5.0 V, V_{IO} = 3.3 V, T_A = 25 °C.

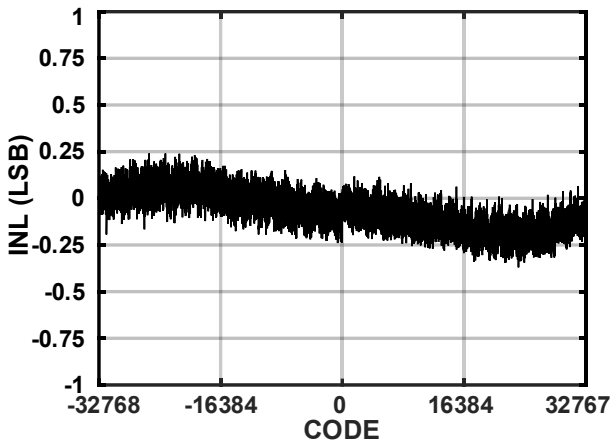

Figure 5. Integral Nonlinearity vs. Code

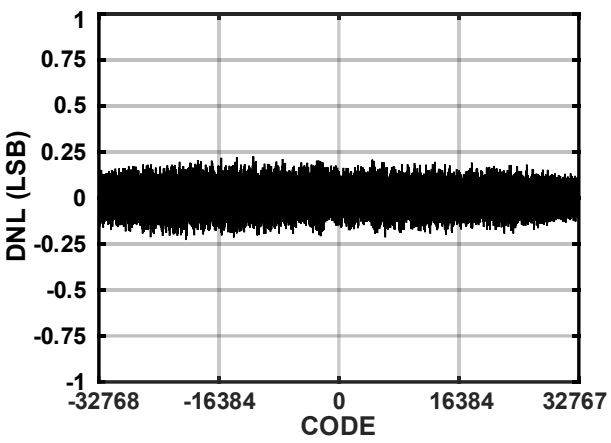

Figure 6. Differential Nonlinearity vs. Code

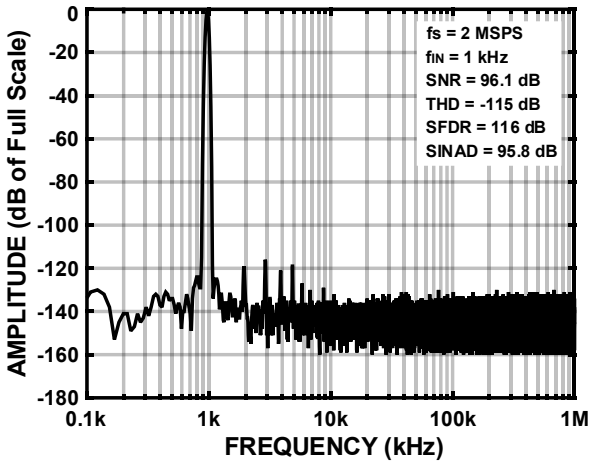

Figure 7. FFT Plot

Theory of Operation

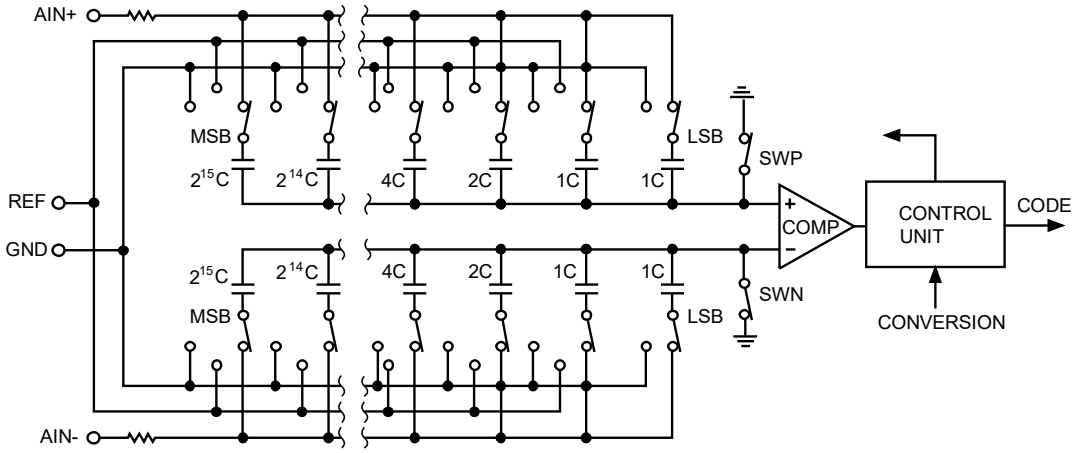

Figure 8. ADC Simplified Circuit Diagram

Circuit Structure

ZJC2400/1-16 is a fast, high precision, low power consumption, 16-bit pseudo differential input successive approximation analog-to-digital converter (SAR ADC). The ZJC2400-16 is capable of converting 2 M samples per second (2 MSPS), with the device entering stand-by mode between conversions, while ZJC2401-16 is capable of converting 1 M samples per second (1 MSPS).

The ZJC2400/1-16 can interface with any 1.8 V to 5 V digital logic level and is available in a 10-lead MSOP package or a 10-lead DFN (LFCSP) package which saves space.

Transfer Function

The ideal transfer function of ZJC2400-16 or ZJC2401-16 is shown in Figure 9.

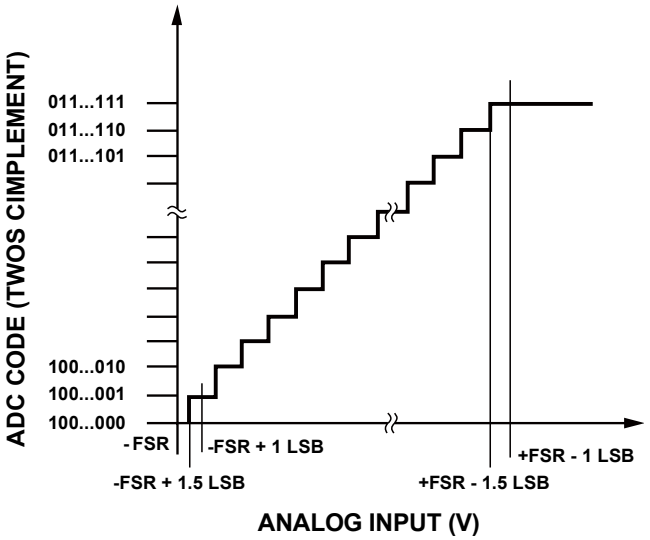

Figure 9. ADC ideal transfer function

Output Code and Ideal Input Voltage:

Description	Analog Input V_{REF} = 5 V	Digital Output (Hex)
FSR - 1 LSB	+4.999847 V	0x7FFF [1]
Midscale + 1 LSB	+153 µV	0x0001
Midscale	0 V	0x0000
Midscale - 1 LSB	-153 µV	0xFFFF
-FSR + 1 LSB	-4.999847 V	0x8001
-FSR	-5 V	0x8000 [2]

[1] This is also the code for an over-range analog input (V_{IN+} − V_{IN-} above V_{REF} − V_{GND}).

[2] This is also the code for an under-ranged analog input (V_{IN+} − V_{IN-} below V_{GND} − V_{REF}).

Typical Connection Diagram

Figure 10 is a suggested connection diagram for the ZJC2400-16 or ZJC2401-16 when multiple power supplies are used.

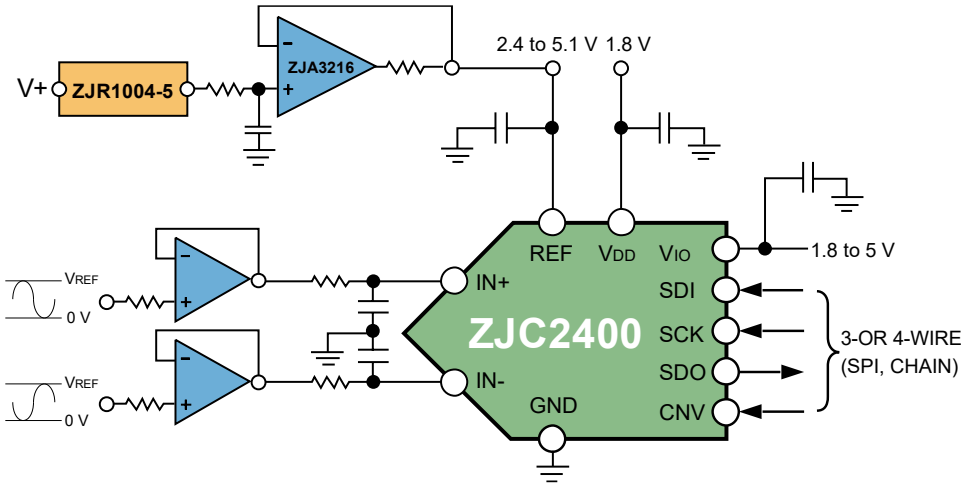

Figure 10. Application Circuits Using Multiple Power Supplies

Figure 11 shows the equivalent circuit of the ZJC2400-16 or ZJC2401-16 input structure.

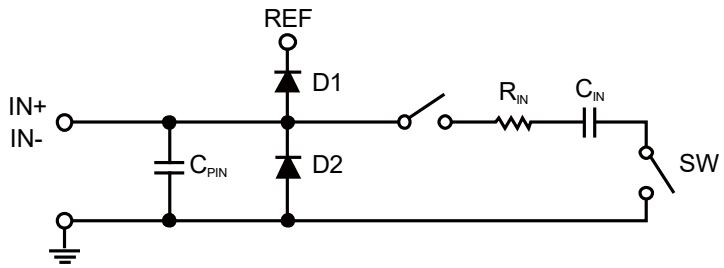

Figure 11. Two Diodes D1 and D2 Provide ESD Protection for the Analog Inputs

Note that the voltage of the analog input signal cannot be higher than the REF voltage by more than 0.3 V. If the voltage of the analog input signal exceeds V_{REF}+0.3 V, the diode will be forward biased and start conducting current. These two diodes can handle forward bias currents up to 50 mA. If the supply voltage of the input driver is higher than V_{REF} the voltage of the analog input signal may be more than 0.3 V higher than the supply voltage. The two diodes D1 and D2 provide ESD protection for analog input IN+ and IN-. The external RC filter, as shown in the Application Circuits above, is usually present at the ADC input to settle the SAR ADC kickback voltage and band limit the input signal. Excessive voltage is dropped across the external resistor, and it becomes part of a protection circuit. The external resistor generally varies from tens of Ω to 1 kΩ for current limit protection.

During the acquisition phase, the impedance of the analog input (IN+) can be seen as the parallel combination of the network formed by R_{IN} and C_{IN} in series and the capacitor C_{PIN}. C_{PIN} mainly includes pin capacitance. R_{IN} typical value is 350 Ω and is a lumped element consisting of the series resistance and the on-resistance of the switch. C_{IN} typical value is 45 pF and consists mainly of the ADC sampling capacitor. High source impedance can significantly affect AC characteristics, especially harmonic distortion. THD degradation is a function of source impedance and analog input frequency.

Single-to-Differential Driver

For applications using single-ended analog signals (bipolar or unipolar), a single-to-differential driver or a dual op amp driver can provide a fully differential input to the ZJC2400/1, see Figure 12 for the schematic diagram.

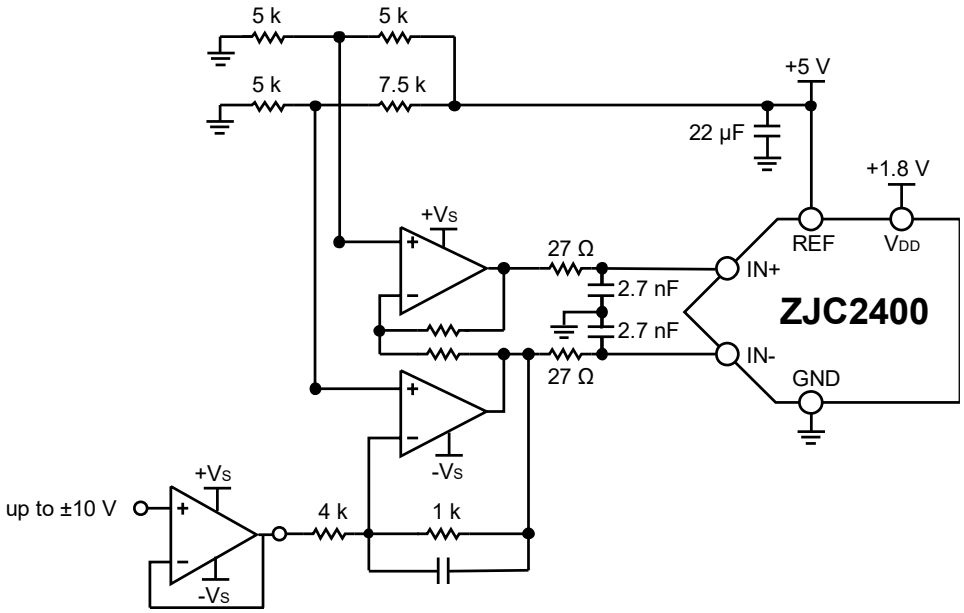

Figure 12. Realizing Bipolar Single-Ended Conversion to Fully differential via Dual Op Amps

A unipolar signal (V_{REF}/2 DC voltage offset) can be buffered and driven back through the op amp to provide a differential input to the ZJC2400/1.

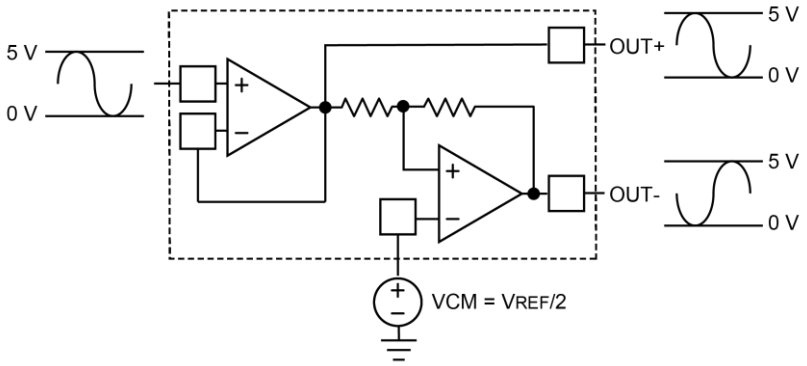

Figure 13. High Input Impedance Unipolar Single-Ended to Fully differential

The fully differential operational amplifier can convert single-ended signals into fully differential signals, and can provide differential input for ZJC2400/1.

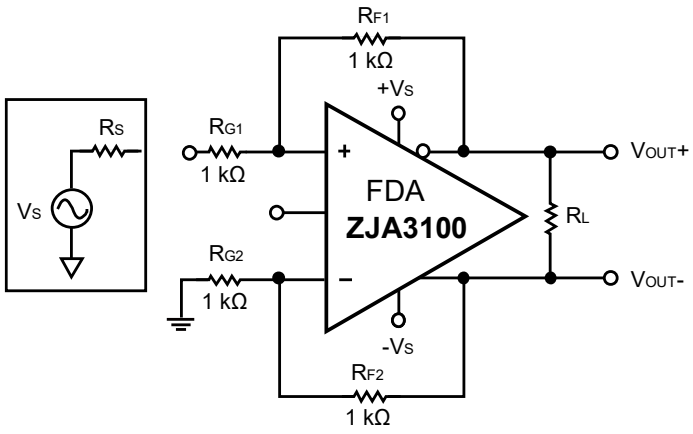

Figure 14. Realizing Bipolar Single-Ended to Fully Differential via Fully Differential Op Amp

If high input impedance is required, an op amp buffer can be added to drive a fully differential op amp. See Figure 15 for the schematic diagram.

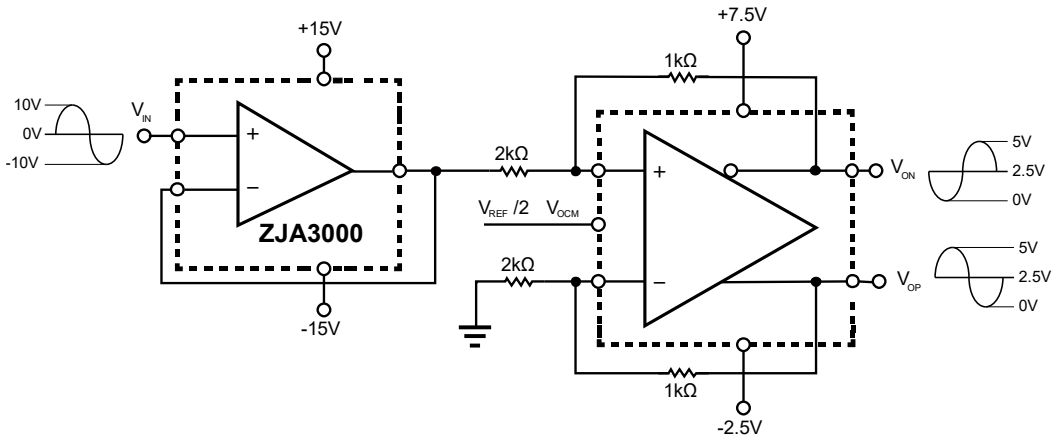

Figure 15. High input impedance bipolar single-ended to fully differential

Reference Voltage Input

For high-precision ADC applications, a precision voltage reference is an essential device. Generally, for 16-bit ADCs, the reference source needs to have low initial error, low noise, and low temperature drift. The ZJC2400/1-16 reference voltage REF has a dynamic input impedance, so it should be driven with a low impedance source. The REF and GND pins should be effectively decoupled as described in the PCB Layout Guidelines section. Figure 16 shows an example of a specific voltage reference and driver design. The ZJR1004 series of high-precision voltage references can just meet these requirements.

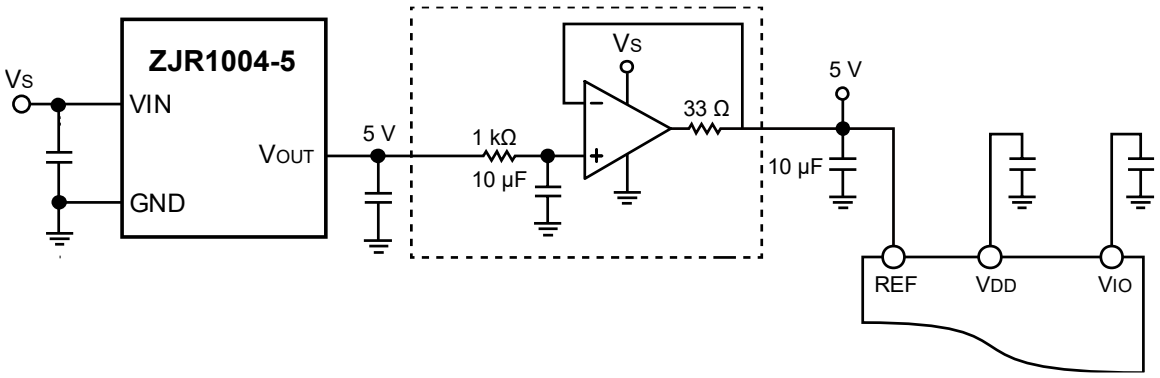

Figure 16. ZJC2400/1-16 Reference Pin Drive

Power Supply

ZJC2400/1-16 uses two power supply pins: core power supply (V_{DD} Normally 1.8 V) and digital input/output interface power supply V_{IO}. V_{IO} can directly interface with any logic from 1.8 V to 5 V.

The ZJC2400/1-16 automatically enters stand-by mode at the end of each conversion stage, so the power consumption is approximately linearly proportional to the sampling rate. This makes the device suitable for low sampling rate and low power consumption applications.

Configuration Register Details

The ZJC2400-16 or ZJC2401-16 has one bit DB[1] in the configuration register for Turbo mode enable or disable.

Bits	Bit Name	Description	Reset
[7:2]	Reserved	Reserved	0x0
[1]	Turbo mode enable	Enables turbo mode: 0: disables turbo mode. 1: enables turbo mode.	0x0
[0]	Reserved	Reserved	0x0

The 16-bit SPI instructions consist of the 8-bit register access command 0x14 (MSB low for write enable and MSB-1 low for write) followed by the configuration register data. When performing register write operation, CNV is analogous to a chip select signal. Data on SDI is latched in on each SCK rising edge. Data is shifted out on SDO on each SCK falling edge.

When performing a write operation, the new register contents are written over SDI, MSB-first, and updated after the device receives the full byte. SPI write instructions can be performed in the same frame as reading a conversion result. To ensure the conversion is executed correctly, the CNV signal must follow the timing requirements for the selected interface mode.

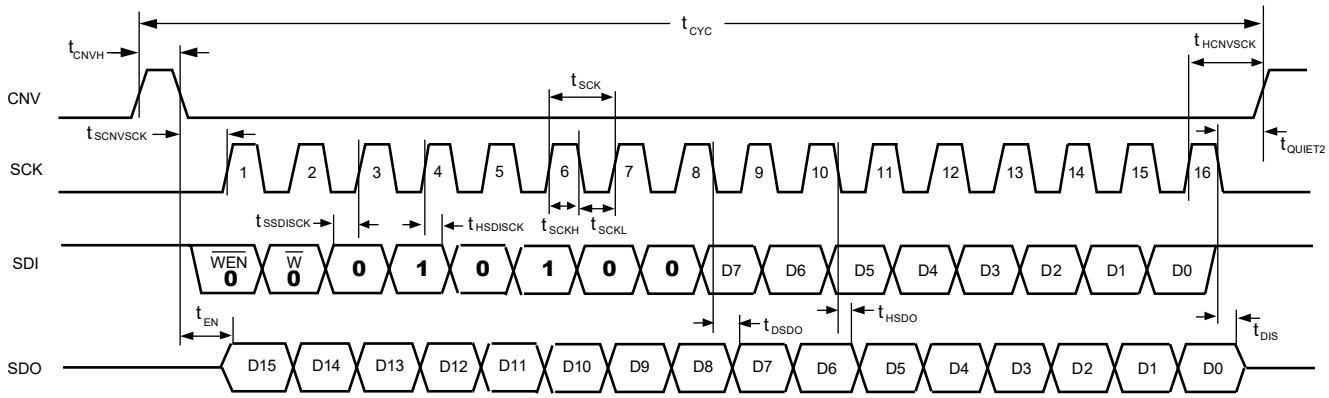

Figure 17. Register Write Timing Diagram

Digital Interface

ZJC2400/1-16 has great flexibility in serial interface mode. In $\overline{CS}$ mode, ZJC2400/1-16 is compatible with SPI, MCU and DSP. In this mode, ZJC2400/1-16 can use 3-wire or 4-wire interface. The 3-wire interface uses CNV, SCK, and SDO signals. The 4-wire interface uses the SDI, CNV, SCK, and SDO signals, with CNV for initiating conversions independent of the read back timing (SDI). In the chain mode, ZJC2400/1-16 provides the daisy chain feature, which allows the cascading of multiple ADCs. If SDI is high, $\overline{CS}$ mode is selected, and if SDI is low, chain mode is selected.

$\overline{CS}$ Mode, 3-Wire Turbo Mode

This mode can be used when ZJC2400/1-16 is connected to a controller which will run at lower SPI clock rate.

In this timing mode, SDI must be high, a rising edge on CNV initiates a conversion, and forces SDO into a high-impedance state. The controller must wait the t_{QUIET1} time after the CNV rising edge before bringing CNV low to read the previous conversion code. When the conversion is complete (after t_{CONV}), the ZJC2400/1-16 enters the acquisition phase and enters the stand-by mode.

When CNV goes low, the MSB is output on SDO. The remaining data bits are clocked out on subsequent falling edges of SCK. After the 16th SCK falling edge, or when CNV goes high (starts next conversion), whichever occurs first, SDO returns to a high-impedance state.

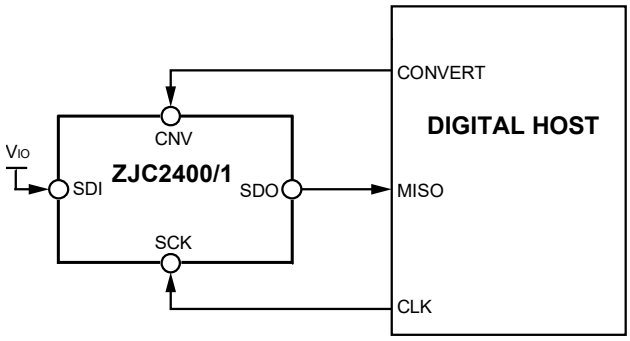

Figure 18. $\overline{CS}$ Mode 3-Wire Turbo Mode Connection Diagram

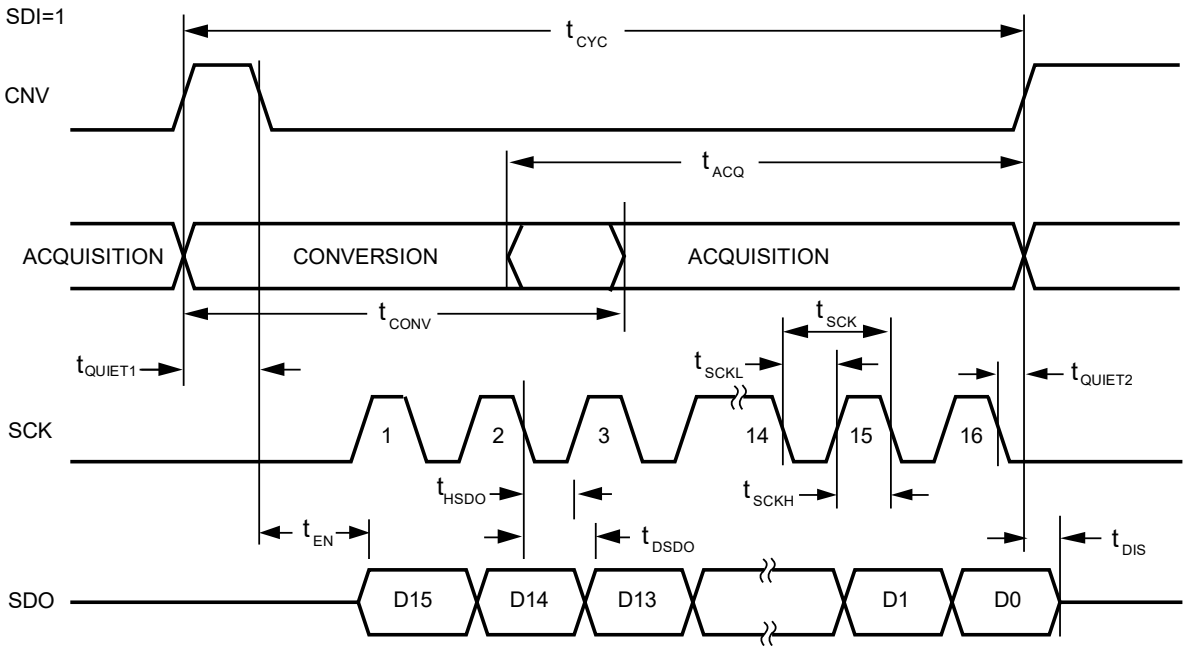

Figure 19. $\overline{CS}$ Mode 3-Wire Turbo Mode Serial Interface Timing

$\overline{CS}$ Mode, 3-Wire without Busy Indication

While SDI is high, a rising edge on CNV initiates a conversion, selects chip-select mode, and forces SDO into a high-impedance state. Once a transition is initiated, the transition will execute to completion regardless of the state of CNV. CNV must return high before the minimum conversion time elapses and then remain high for the maximum possible conversion time to avoid generating a busy signal indication. After the conversion is completed, the ZJC2400/1-16 enters the acquisition phase and enters the stand-by mode.

When CNV goes low, the MSB is output on SDO. The remaining data bits are clocked out on subsequent falling edges of SCK. After the 16th SCK falling edge, or when CNV goes high, whichever occurs first, SDO returns to a high-impedance state.

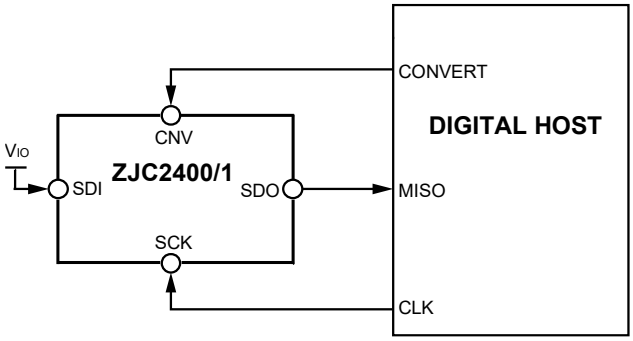

Figure 20. $\overline{CS}$ Mode (3-wire without Busy Indication) Connection Diagram

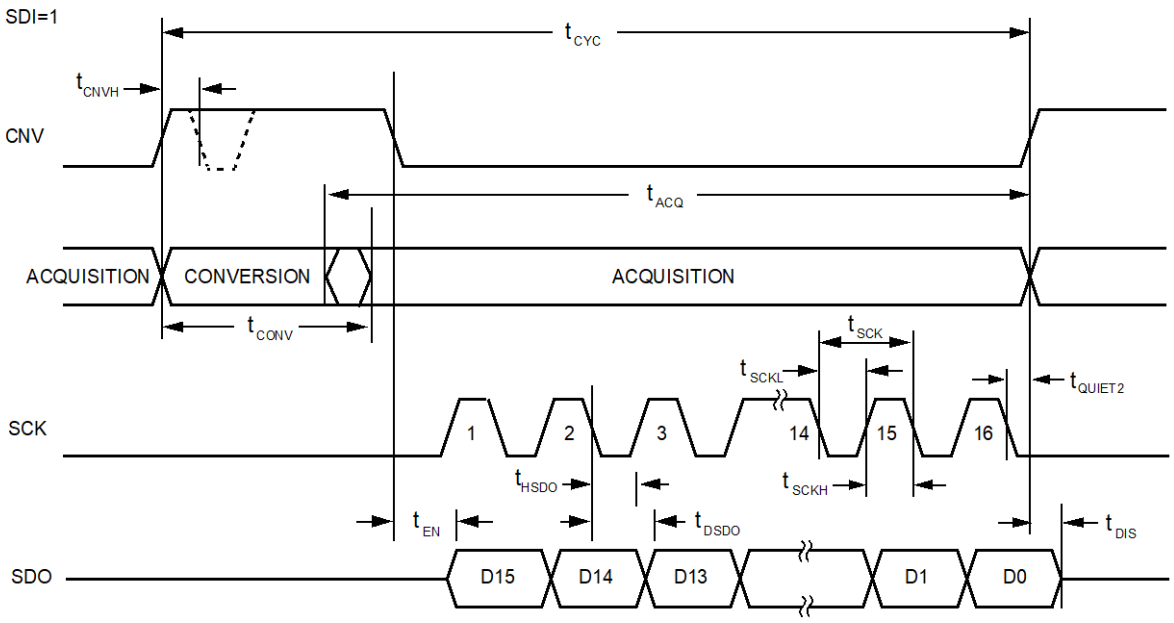

Figure 21. $\overline{CS}$ Mode (3-Wire without Busy Indication) Serial Interface Timing

$\overline{CS}$ Mode, 3-Wire with Busy Indication

When connecting SDI to VIO, a rising edge on CNV initiates a conversion, selects $\overline{CS}$ mode, and forces SDO into a high-impedance state. Regardless of the state of CNV, SDO remains high impedance until the conversion is complete. CNV must return to low before the minimum transition time has elapsed and then remain low for the maximum possible transition time to guarantee a busy signal indication. When the transition is complete, SDO changes from a high-impedance state to a low-impedance state. Combined with a pull-up resistor on the SDO line, this transition can be used as an interrupt signal. Next ZJC2400/1-16 enters the acquisition stage and enters the stand-by mode. Data bits are clocked out on subsequent falling edges of SCK, MSB first. After the optional 17th SCK falling edge, or when CNV goes high, whichever occurs first, SDO returns to a high-impedance state.

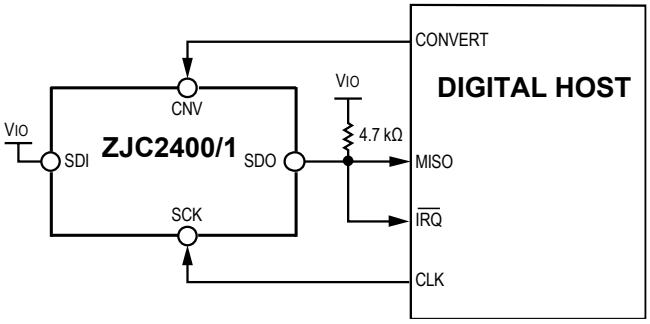

Figure 22. Chip select mode (3-wire type with busy indication) connection diagram

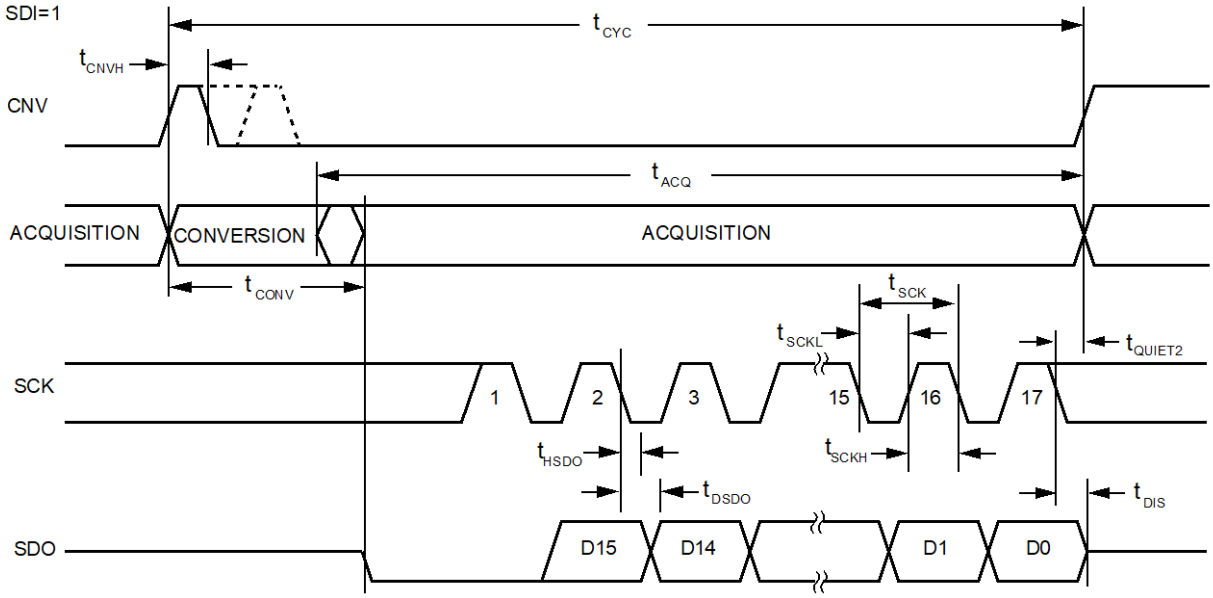

Figure 23. $\overline{CS}$ Mode (3-Wire with Busy Indication) Serial Interface Timing

$\overline{CS}$ Mode, 4-Wire Turbo Mode

This mode can be used when ZJC2400/1-16 is connected to a controller which will run at lower SPI clock rate, and use SDI as a dedicated $\overline{CS}$ pin.

A rising edge on CNV initiates a conversion, and forces SDO into a high-impedance state. CNV must be held high throughout the conversion and code read-back phase, and SDI must be high during the CNV rising edge. The controller must wait the t_{QUIET1} time after the CNV rising edge before bringing SDI low to read the previous conversion code. When the conversion is complete (after t_{CONV}), the ZJC2400/1-16 enters the acquisition phase and enters the stand-by mode.

SDI is used as a chip select input, and bringing SDI low outputs the MSB of the conversion result on SDO. The remaining data bits are clocked out on subsequent falling edges of SCK. After the 16th SCK falling edge, or when SDI goes high, whichever occurs first, SDO returns to a high-impedance state.

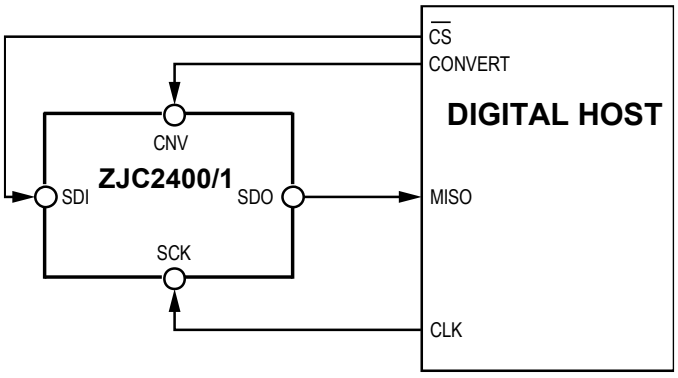

Figure 24. $\overline{CS}$ Mode (4-wire without Busy Indication) Connection Diagram

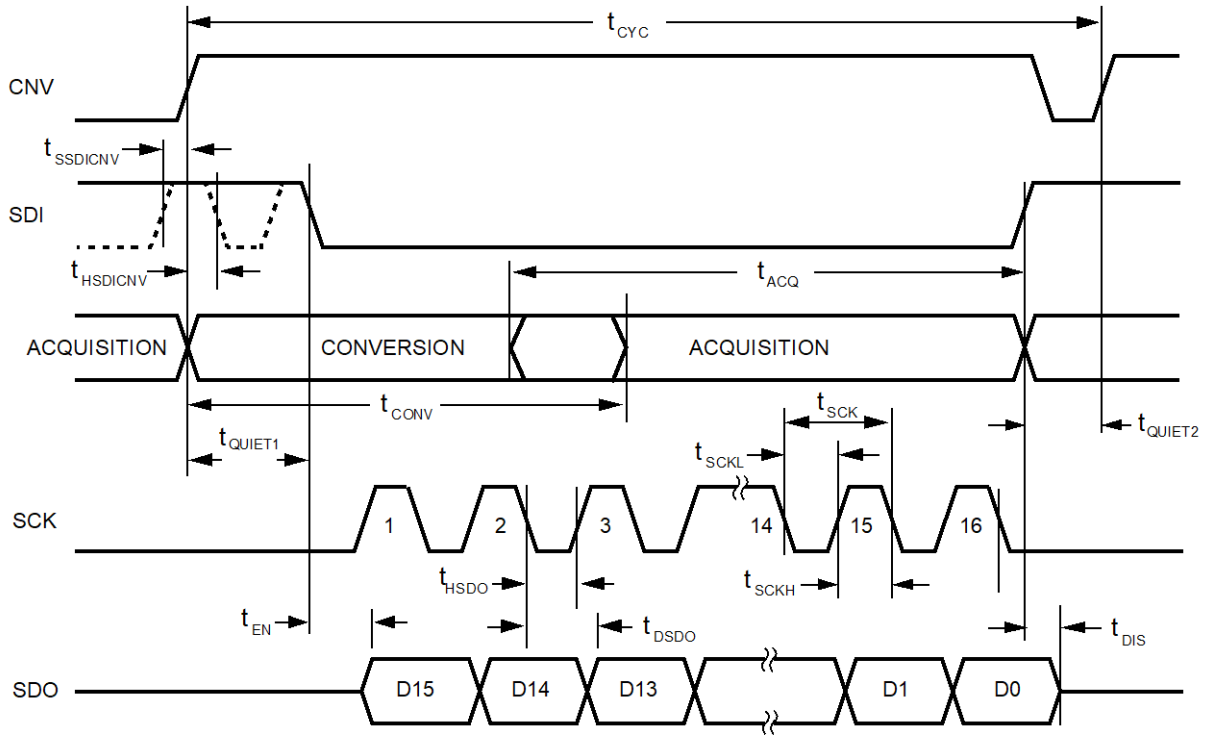

Figure 25. $\overline{CS}$ Mode (4-Wire without Busy Indication) Serial Interface Timing

$\overline{CS}$ Mode, 4-wire without Busy Indication

With SDI high, a rising edge on CNV initiates a conversion, selects $\overline{CS}$ mode, and forces SDO into a high-impedance state. In this mode, CNV must be held high during the conversion phase and subsequent data readback. If SDI and CNV are low, SDO goes low.

SDI must keep or return high before the minimum transition time elapses and then remain high for the maximum possible transition time to avoid generating a busy signal indication. After the conversion is completed, the ZJC2400/1-16 enters the acquisition phase and enters the stand-by mode. Each ADC converted code value can be read by pulling the SDI input low, which outputs the MSB to SDO. The remaining data bits are clocked out on subsequent SCK falling edges. After the 16th SCK falling edge, or when SDI goes high, whichever occurs first, SDO returns to high impedance and another ZJC2400/1-16 can be read.

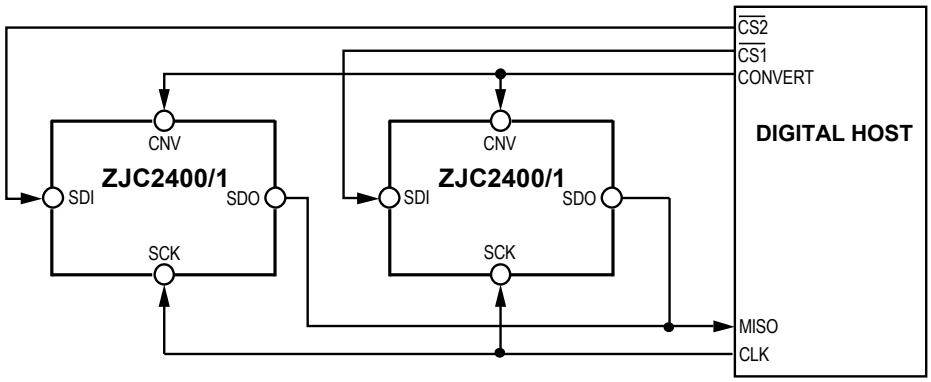

Figure 26. $\overline{CS}$ Mode (4-wire without Busy Indication) Connection Diagram

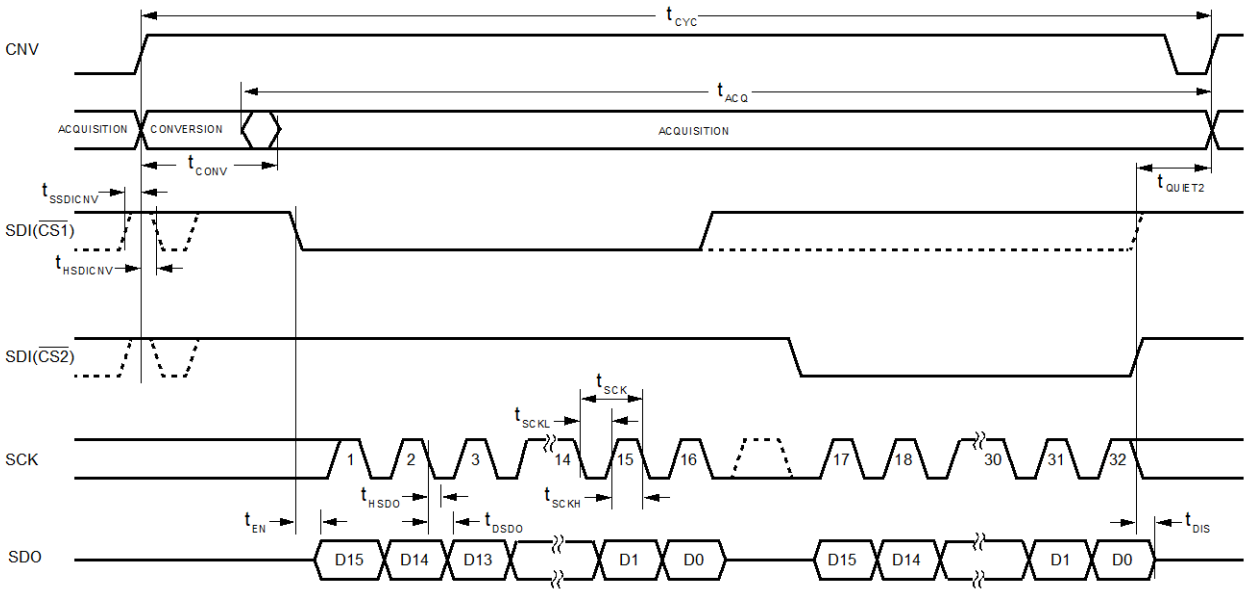

Figure 27. $\overline{CS}$ Mode (4-Wire without Busy Indication) Serial Interface Timing

$\overline{CS}$ Mode, 4-Wire with Busy Indication

With SDI high, a rising edge on CNV initiates a conversion, selects $\overline{CS}$ mode, and forces SDO into a high-impedance state. In this mode, CNV must be held high during the conversion phase and subsequent data readback. If SDI and CNV are low, SDO goes low. SDI must return low before the minimum transition time elapses and then remain low for the maximum possible transition time to guarantee a busy signal indication. When the transition is complete, SDO changes from a high-impedance state to a low-impedance state. Combined with a pull-up resistor on the SDO line, this transition can be used as an interrupt signal to initiate data readback. Next, ZJC2400/1-16 enters the acquisition phase and is on stand-by. Data bits are clocked out on subsequent falling edges of SCK, MSB first. After the optional 17th SCK falling edge or after SDI goes high, whichever occurs first, SDO returns to a high-impedance state.

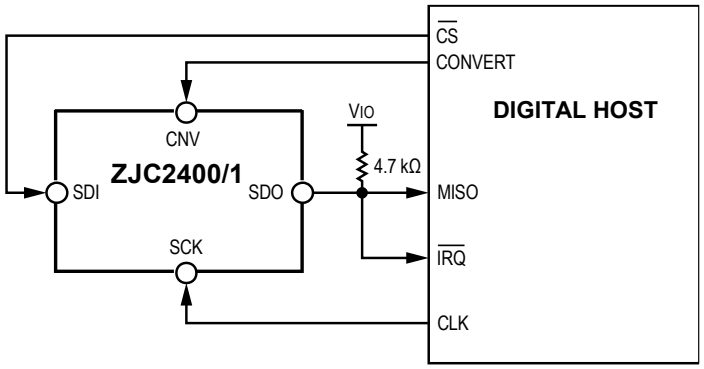

Figure 28. CS Mode (4-Wire with Busy Indication) Connection Diagram

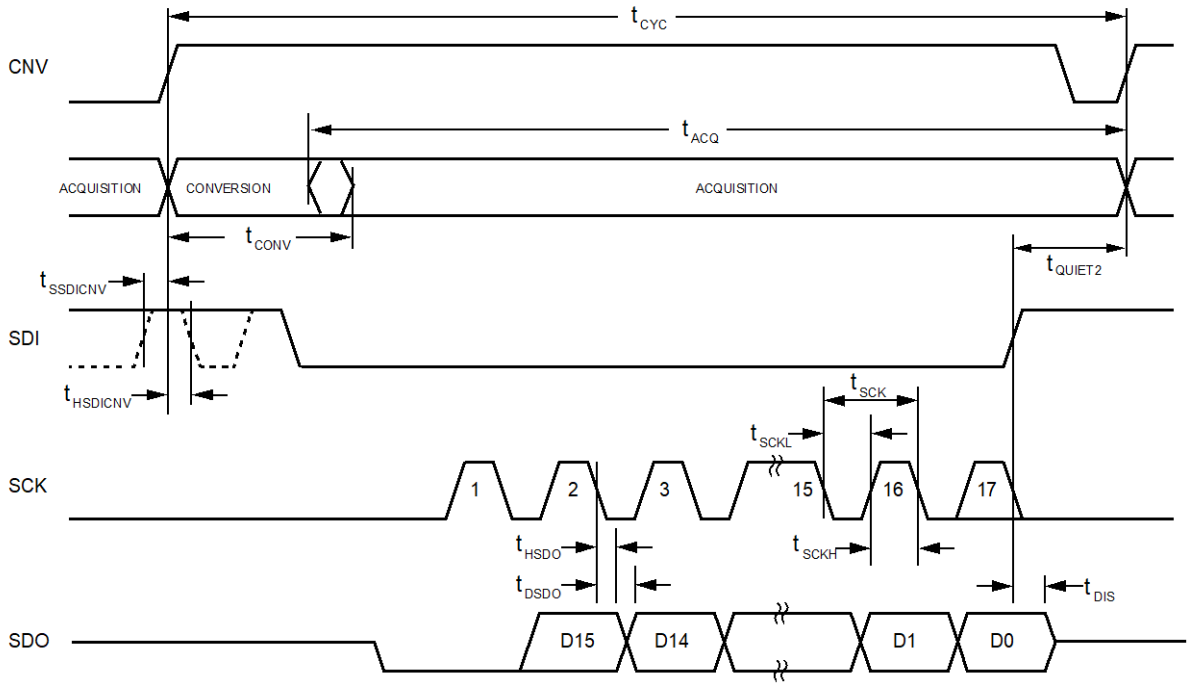

Figure 29. CS Mode (4-wire with Busy Indication) Serial Interface Timing

Chain Mode, without Busy Indication

This mode can be used to daisy-chain multiple ZJC2400/1-16s over a serial interface. An example using two ZJC2400/1-16s is shown in Figure 30, and the corresponding timing is shown in Figure 31.

When SDI and CNV are low, SDO goes low. With SCK low, a rising edge on CNV initiates a conversion, selects chain mode, and disables the busy indication. In this mode, CNV remains high during the conversion phase and subsequent data readback. After the conversion is completed, the MSB is output to SDO, and ZJC2400/1-16 enters the acquisition phase and stands by. The remaining data bits stored in the internal shift register are clocked out on subsequent SCK falling edges. For each ADC, SDI feeds the input of the internal shift register and is clocked out by SCK falling edge. Each ADC in the chain outputs the data MSB first, and it takes 16×N clocks to read back N ADCs.

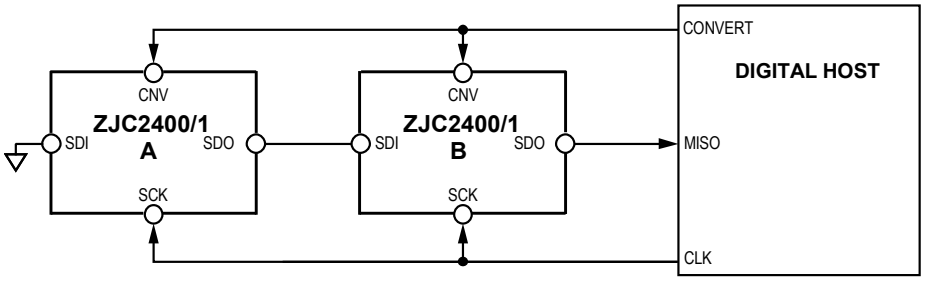

Figure 30. Chain Mode (without Busy Indication) Connection Diagram

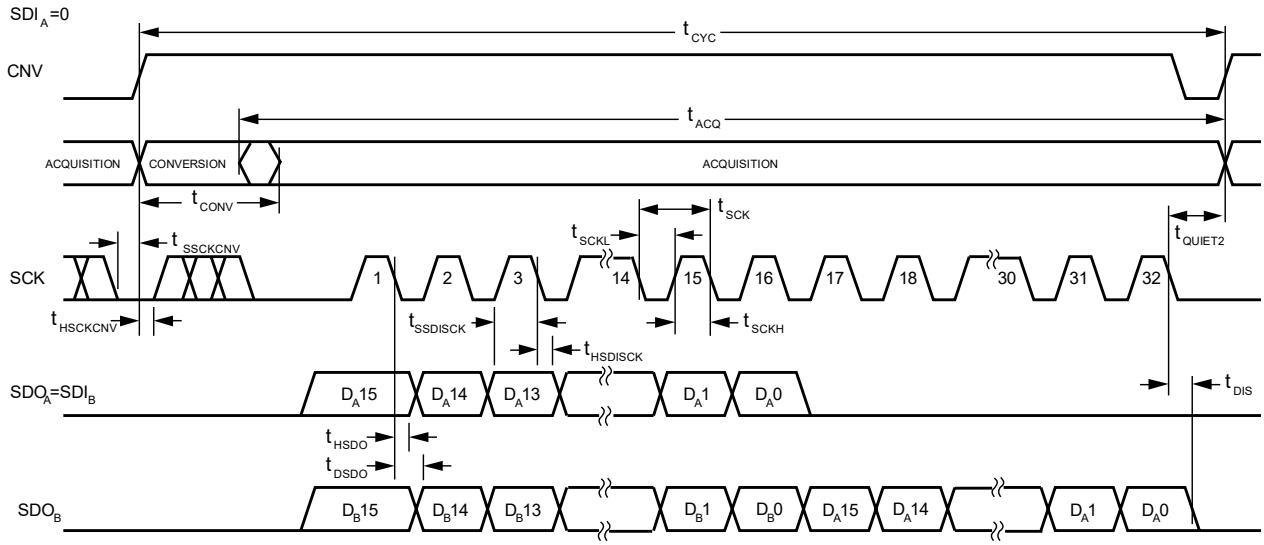

Figure 31. Chain Mode (without Busy Indication) Serial Interface Timing

Layout Guidelines

For optimum performance of the device, good PCB layout practices are recommended, including:

- It is recommended that to use a design that separates the analog part and the digital part on the ZJC2400/1-16 PCB, and each is limited to a certain area of the circuit board.
- Avoid running digital lines under the device, which may couple noise onto the die, unless a ground plane under the ZJC2400/1-16 is used as a shield. Fast switching signals such as CNV or clocks should not be placed close to the analog signal path. Crossover of digital and analog signals should be avoided.
- At least one ground plane should be used. It can be common or split between the digital and analog sections. In the latter case, the planes should be joined close to the ZJC2400/1-16.
- The ZJC2400/1-16 voltage reference input, REF, has a dynamic input impedance and should be decoupled with one 10 µF ceramic capacitors to minimize parasitic inductances. This is done by placing the reference decoupling ceramic capacitor close to, ideally right up against, the REF and GND pins and connecting them with wide, low impedance trace
- The power supply V_{DD} of ZJC2400/1-16 should be decoupled with 10 µF and 100 nF ceramic capacitors, placed close to the ZJC2400/1-16 and connected using short, wide traces to provide low impedance paths and to reduce the effect of noises on the power supply lines.

Figure 32 is an example of the guidance.

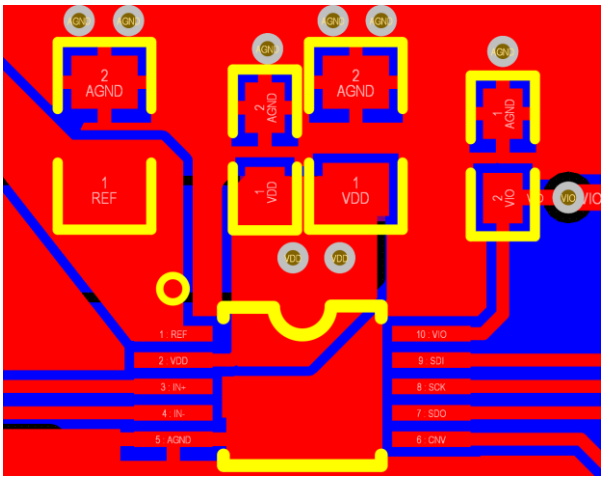

Figure 32. Example Layout and Routing of ZJC2400

Outline Dimensions

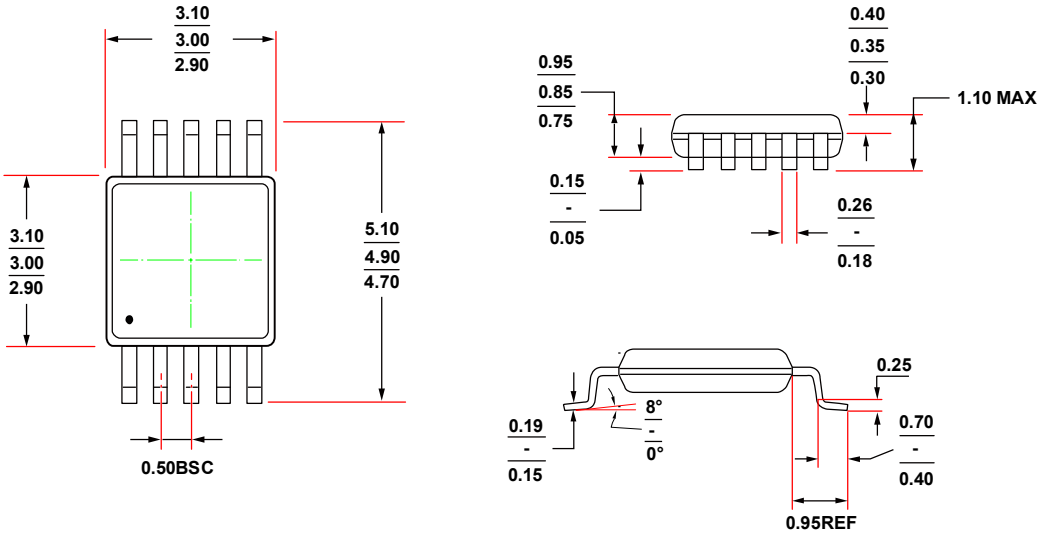

Figure 33. 10-Lead MSOP Package Dimensions shown in millimeter

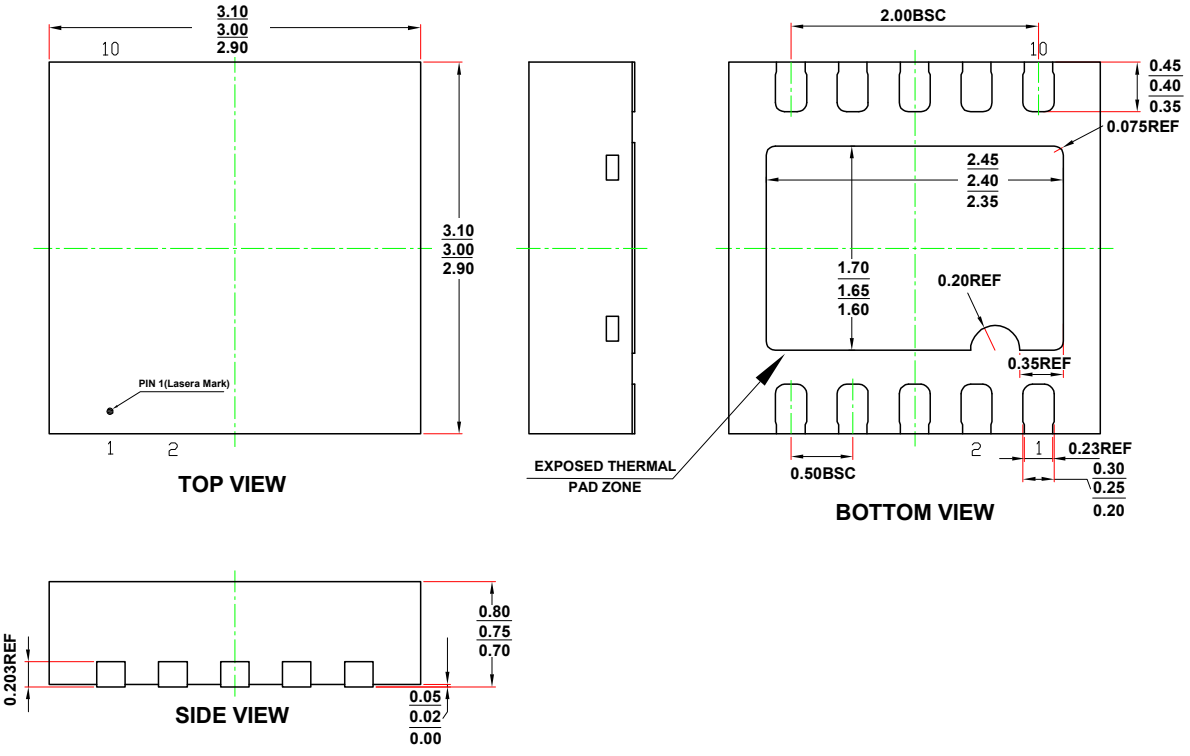

Figure 34. 10-Lead DFN Package Dimensions shown in millimeter

Ordering Guide

Model	Orderable Device	Resolution (bit)	Supply Voltage (V)	Temperature Range (°C)	Package	External Package
ZJC2400-16	ZJC2400-16AUBBT	16	1.71 to 1.89	-40 to +125	MSOP-10	Tube
	ZJC2400-16AUBBR				MSOP-10	13” Reel
	ZJC2400-16ATBBR				DFN-10	13” Reel
ZJC2401-16	ZJC2401-16AUBBT	16	1.71 to 1.89	-40 to +125	MSOP-10	Tube
	ZJC2401-16AUBBR				MSOP-10	13” Reel
	ZJC2401-16ATBBR				DFN-10	13” Reel

Product Order Model

ZJXXXXX X X X X X Q1

- Q1: Automotive Grade
- External Package: T = Tube; R = Reel
- Temperature Range: A = -40 °C to 125 °C Automotive Grade 1, B = -40 °C to 125 °C; E = -40 °C to 85 °C
- Number of Pins: R = 3; K =5; T = 6, A = 8; B = 10; D = 14; E = 16; P = 20
- Package Type: S = SOIC; U = MSOP, TSSOP, SOT; T = DFN, QFN; X = SC70; W = WLCSP; Z = TSOT23
- Grade: B grade is better than A grade
- Base: R = Voltage reference; A = Amplifier; C = Data Converter; G = Switches and Multiplexers; M = Others

Related Parts

Part Number	Description	Comments
ADC		
ZJC2020	20-bit 350 kSPS SAR ADC	Fully differential input, SINAD 101.4 dB, THD -118 dB
ZJC2000/2010	18-bit 400 kSPS/200 kSPS SAR ADC	Fully differential input, SINAD 99.3 dB, THD -113dB
ZJC2001/2011	16-bit 500 kSPS/250 kSPS SAR ADC	Fully differential input, SINAD 95.3 dB, THD -113 dB
ZJC2002/2012 ZJC2003/2013	16-bit 500 kSPS/250 kSPS SAR ADC	Pseudo-differential unipolar input, SINAD 91. 7 dB, THD -105 dB Pseudo-differential bipolar input, SINAD 91.7 dB, THD -105 dB
ZJC2004/2014 ZJC2005/2015	18-bit 400 kSPS/200 kSPS SAR ADC	Pseudo-differential unipolar input, SINAD 94.2 dB, THD -105 dB Pseudo-differential bipolar input, SINAD 94.2 dB, THD -105 dB
ZJC2007/2017 ZJC2008/2018	14-bit 600 kSPS/300 kSPS SAR ADC	Pseudo-differential unipolar input, SINAD 85 dB, THD -105 dB Pseudo-differential bipolar input, SINAD 85 dB, THD -105 dB
ZJC2100/1-18 ZJC2100/1-16	18-bit 400 kSPS/200 kSPS 4-ch differential SAR ADC, SINAD 99.3 dB, THD -113 dB 16-bit 500 kSPS/250 kSPS 4-ch differential SAR ADC, SINAD 95.3 dB, THD -113 dB	
ZJC2102/3-18 ZJC2102/3-16 ZJC2102/3-14	18-bit 400 kSPS/200 kSPS 8-ch pseudo-differential SAR ADC, SINAD 94.2 dB, THD -105 dB 16-bit 500 kSPS/250 kSPS 8-ch pseudo-differential SAR ADC, SINAD 91.7 dB, THD -105 dB 14-bit 600 kSPS/300 kSPS 8-ch pseudo-differential SAR ADC, SINAD 85 dB, THD -105 dB	
ZJC2104/5-18 ZJC2104/5-16	18-bit 400 kSPS/200 kSPS 4-ch pseudo-differential SAR ADC, SINAD 94.2 dB, THD -105 dB 16-bit 500 kSPS/250 kSPS 4-ch pseudo-differential SAR ADC, SINAD 91.7 dB, THD -105 dB	
DAC		
ZJC2541-18/16/14 ZJC2543-18/16/14	18/16/14-bit 1 MSPS single channel DAC with unipolar output	Power on reset to 0 V (ZJC2541) or V_{REF}/2 (ZJC2543), 1 nV-S glitch, SOIC-8, MSOP-10/8, DFN-10 packages
ZJC2542-18/16/14 ZJC2544-18/16/14	18/16/14-bit 1 MSPS single channel DAC with bipolar output	Power on reset to 0 V (ZJC2542) or V_{REF}/2 (ZJC2544), 1 nV-S glitch, SOIC-14, TSSOP-16, QFN-16 packages
Amplifier		
ZJA3000-1/2/4 ZJA3001-1/2/4	Single/Dual/Quad 36 V low bias current precision Op Amps	3 MHz, 35 µV max Vos, 0.5 µV/°C max TCVos, 25 pA max Ibias, 1 mA/ch, input to V- (ZJA3000 only), RRO, 4.5 V to 36 V
ZJA3018-2 ZJA3008-2	OVP ±75V, 36 V, Low Power, High Precision Op Amp 36 V, Low Power, High Precision Op Amp	1.3 MHz, 10 µV max Vos, 0.5 µV/°C max TCVos, 25 pA max Ibias, 0.5 mA/ch, OVP±75 V (ZJA3018 only), RRO, 4.5 V to 36 V
ZJA3512-2	Dual 36 V 7 MHz precision JFET Op Amps	7 MHz, 35 V/µS, 50 µV max Vos, 1 µV/°C max TCVos, 2 mA/ch, RRO, 9 V to 36 V
ZJA3216/06/02-1/2	Precision 20/11.6/5.3 MHz CMOS RRIO Op Amps	20/11.6/5.3 MHz, RRIO, 30 µV max Vos, 1 µV/°C max TCVos, 0.6 pA Ib, 2.7 V to 5.5 V
ZJA3600/1	36 V ultra-high precision in-amp	CMRR 105 dB min (G=1), 25 pA max Ib, 25 µV max Vosi, ±2.4 V to ±18 V, -40°C to 125°C
ZJA3611, ZJA3609	36 V precision wider bandwidth precision in-amp (G≥10)	CMRR 120 dB min (G=10), 25 pA max Ibias, 25 µV max Vosi, 1.2 MHz BW (G=10)
ZJA3676/7 ZJA3678/9	Low power, G=1 Single/Dual 36 V difference amplifier Low power, G=0.5/2 Single/Dual 36 V difference amplifier	Input protection to ±65 V, CMRR 104 dB min (G=1), Vos 100 µV max, gain error 15 ppm max, 500 kHz BW (G=1), 330 µA/channel, 2.7 V to 36 V
ZJA3669	High Common-Mode Voltage Difference Amplifier	±270 V CMV, 2.5 kV ESD, 96 dB min CMRR, 450 kHz BW, 4 V to 36 V, SOIC-8
ZJA3100	15 V precision fully differential amplifier	145 MHz, 447 V/µS, 50 nS to 16-bit, 50 µV max Vos, 4.6 mA Iq, SOIC/MSOP-8, QFN-16
ZJA3236/26/22-2	Low-cost 22/10/5 MHz CMOS RRIO Op Amps	22/11/5 MHz, RRIO, 2 mV max Vos, 6 µV/°C max TCVos, 0.6 pA Ib, 2.7 V to 5.5 V
ZJA3622/8	36 V low-cost precision in-amp	0.5 nA max Ibias, 125 µV max Vosi, 625 kHz BW (G=10), 3.3 mA Iq, ±2.4 V to ±18 V
Voltage Reference		
ZJR1004	40 V supply precision voltage reference	V_{OUT}=2.048/2.5/3/3.3/4.096/5/10 V, 5 ppm/°C max drift -40°C to 125°C
ZJR1001/2 ZJR1003	5.5 V low power voltage reference (ZJR1001 with noise filter option)	V_{OUT}=2.048/2.5/3/3.3/4.096/5 V, 5 ppm/°C max drift -40°C to 125°C, ±0.05% initial error, 130 µA, ZJR1001/2 in SOT23-6, ZJR1003 in SOIC/MSOP-8
Switches and Multiplexers		
ZJG4438/4439	36 V fault protection 8:1/dual 4:1 multiplexer	Protection to ±50 V power on&off, latch-up immune, Ron 270 Ω,14.8 pC, t_{ON} 166 nS
ZJG4428/4429	36 V 8:1/dual 4:1 multiplexer	Latch-up immune, Ron 270 Ω,14.8 pC charge injection, t_{ON} 166 nS
Quad Matching Resistor		
ZJM5400	±75 V precision match resistors	Mismatch<100 ppm, 10k:10k:10k:10k, 100k:100k:100k:100k, 100k:10k:10k:100k, 1k:1k:1k:1k, 1M:1M:1M:1M, 5k:1k:1k:5k, 5k:1.25k:1.25k:5k, 9k:1k:1k:9k, ESD: 3.5 kV